28.5 A 1/2.5 inch 8.1Mpixel CMOS Image Sensor for Digital Cameras

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This paper presents a 1/2.5 inch format 8.1Mpixel CMOS active-pixel digital image sensor that targets both mobile and digital still-camera (DSC) applications. The chip incorporates sophisticated camera functions such as windowing, mirroring, column/row binning and skip modes, down-size scaling, global shutter and snapshot mode. It is programmable through a simple two-wire serial interface. The image sensor is designed to operate at 2.8V for DSC applications and supports flash and mechanical shutter actuators. It can operate down to 2.4V in mobile applications. The imager includes a low-noise signal readout chain, a 12b analog-to-digital converter (ADC), an internal phase-locked loop (PLL) and a 12b parallel interface to output pixel data at up to 96 Megapixels per second (Mp/s).

The imager uses a 1.75μm×1.75μm 1.75T-cell pixel configured in a common element pixel architecture (CEPA) for high fill factor and light sensitivity. The chip uses top and bottom multiple channels with a double-data-rate analog signal readout at a rate of 96Mp/s, which results in 15 frames per second (fps) at full resolution and 30fps at VGA resolution in full field of view (FOV). Operating power consumption of the chip in full resolution at 11fps is less than 400mW and, with dynamic power management, a reduction of more than 30% of the total power is achieved by turning off analog blocks for a period of time when they do not operate [1]. In standby mode, measurments show that the imager draws less than 20μA. The imager is fabricated in a standard 0.13μm CMOS process. The chip dimensions are 7.86mm×7.75mm.

Figure 28.5.1 shows the block diagram of the imager. The default 8M active imager area is 3,264(H)×2,448(V) for a 1/2.5 inch optical format. The chip uses top and bottom readout analog signal chains to read odd and even columns for each color, respectively. Each of the top or bottom readout signal chains uses a double data-rate analog signal chain architecture. Thus the clock frequency for each of the analog signal chains is only a quarter of the master input clock while yielding true 11b ADC accuracy in terms of differential non-linearity (DNL). The two programmable gain amplifiers (PGA) in front of the ADC use single-stage high-speed gain-boosting folded-cascode topologies in order to achieve high DC gain with high unity-gain frequency and obtain better gain linearity, matching and a large enough output swing at 2.4V [2].

A high-level signal-flow block diagram of the imager data path is shown in Fig. 28.5.2. Each color is processed independently, including separate gain and offset controls. Output voltages sampled from the pixel array are first passed through PGA stage 1 and 2, which can produce gain factors from 1 through 15.875. Then there are 4 main algorithms determining the black level in the output image. First, there is an analog offset calibration to compensate for analog offset and ensure that the ADC range is utilized well. This calibration is accomplished by injecting an analog voltage into the analog signal chain in front of the ADC. Second, row noise correction plays two roles in the sensor: It reduces row noise in the image; and it fine-adjusts the black level. The second role is important since the analog offset calibration can settle on slightly different values for different colors due to inaccuracies. Third, there is dark current compensation to compensate for the dark current, and the digital gain can be set independently for each color; the gain must be a whole number in the range 1 to 7. The black level will not change during this operation since the mean level is 0 at this point in the data path. Fourth, the data pedestal is a programmable value applied to all active pixels in a frame to avoid clipping at zero. The default value is 168 for a 12b sensor. The resulting 12b pixel value is then transferred to the DOUT[11:0] output ports.

Figure 28.5.3 shows a block diagram of the double-data-rate analog signal chain in which each clock cycle is used to acquire two samples and perform two conversions. The fully differential operational amplifier converts the signal during both phases of the clock. Hence, DC-bias current is not wasted during the sampling phase of the operation [3]. In effect, the throughput of each stage is doubled for a given DC-bias current consumption. Capacitor matching in the process is adequate to achieve 12 bits of accuracy without digital correction.

Figure 28.5.4 shows the 1.75T/pixel CEPA structure. In this topology, one floating diffusion (FD) is shared by four pinned photodiodes (PPD) to maximize the active area (AA) fill factor. During the pixel readout operation, one line of buffer memory is needed for the reordering operation and three different charge pumps are used to boost the voltages of the reset (RST), transfer (TX), and row-select (ROW) signals to a programmable voltage higher than the pixel-array supply voltage (VAAPIX) [4].

The conversion gain of 101μV/e^- is achieved by setting the FD capacitor to 1.6fF. The dark current is 6.1e^-/s at 30°C. The full well capacity is over 7,000 electrons and the measured maximum SNR is 36.0dB. With unity analog gain, the noise floor is equal to 8.2e^- rms. With the analog gain set to 15.875×, the noise floor falls as low as 3.8e^-, providing a pixel dynamic range of 63.8dB. The dark signal non-uniformity (DSNU) at 35°C is measured to be 0.033% of full well, and photo-response non-uniformity (PRNU) is measured to be 1.00% at 50% saturation in green pixels. Figure 28.5.5 shows a sample image taken with the D65 light condition. Key parameters are summarized in Fig. 28.5.6. The chip micrograph is shown in Fig. 28.5.7.

The 8.1Mpixel CMOS imager presented in this paper is suitable for both digital still camera and mobile applications. The measured read noise and low-light performance prove that this CMOS imager represents the state-of-the-art and outperforms CCDs with the same optical format. The imager achieves better than CCD image quality based on signal-to-noise ratio and low-light sensitivity while maintaining the inherent size, cost, power consumption, and integration advantages of CMOS.

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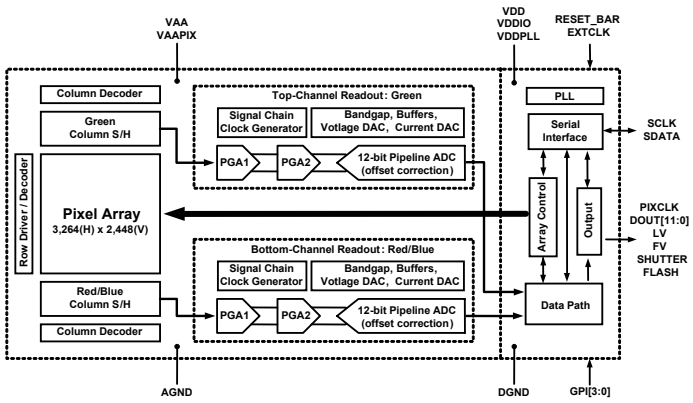

Figure 28.5.1: Block diagram.

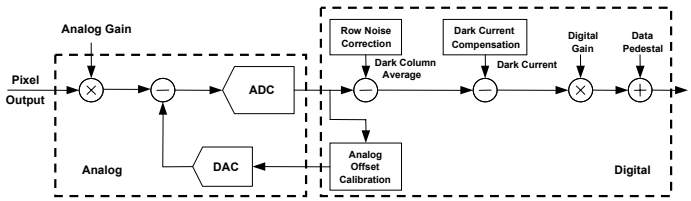

Figure 28.5.2: High-level signal-flow block diagram of data path.

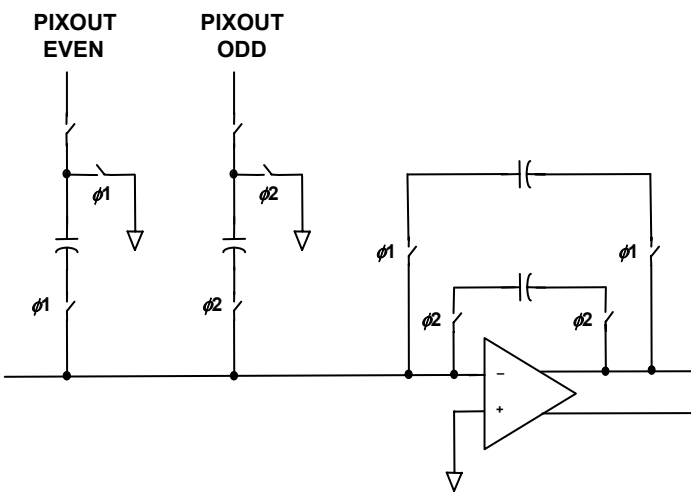

Figure 28.5.3: Block diagram of the double-data-rate analog signal chain front end.

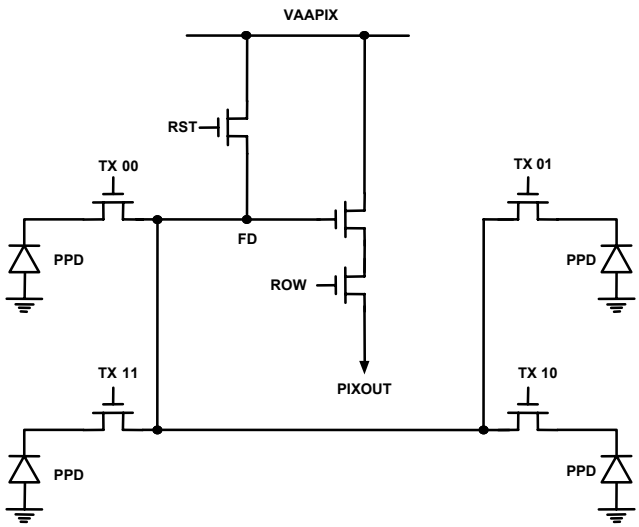

Figure 28.5.4: 1.75T/pixel common element pixel architecture (CEPA).

Figure 28.5.5: Sample image taken with the D65 light condition.

Conversion gain @ FD (μV/e-)	101
Responsivity @ FD (V/Lux·sec)	0.48
Read noise at 1× gain (e-)	8.2
Read noise at 15.875× gain (e-)	3.8
PRNU @ 50% saturation, green pixels at 550nm (%)	1.00
DSNU @ 35C (% of full well)	0.033
Total SNR max, green pixels (dB)	36
Saturation full well (e-)	7208
Pixel dynamic range (dB)	63.8
Mean dark current @ 30°C (e-/sec)	6.1

Figure 28.5.6: Key parameters.

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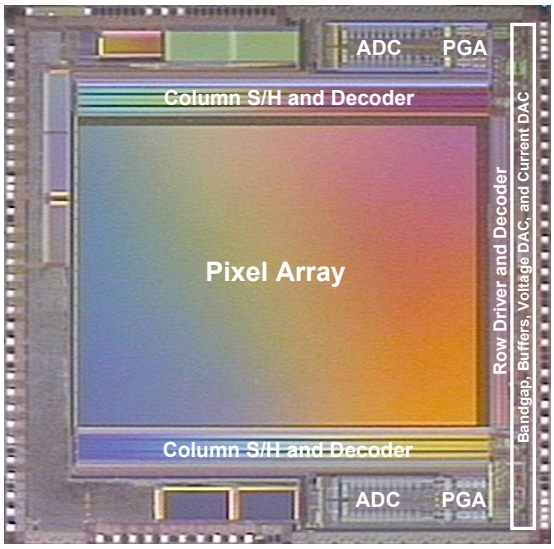

Figure 28.5.7: Chip micrograph.

